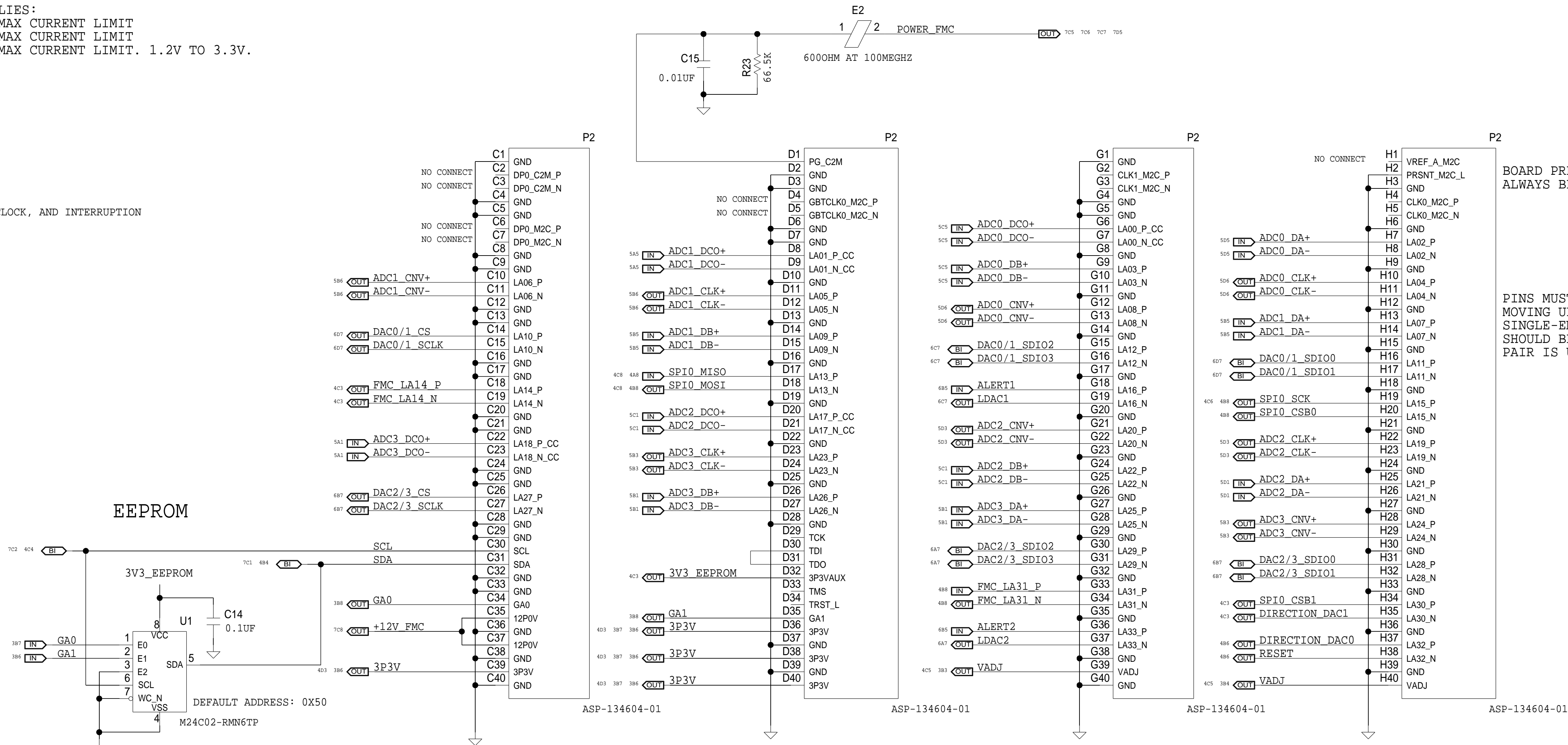


FPGA FMC CONNECTIONS

POWER SUPPLIES:
12P0V. 1A MAX CURRENT LIMIT
3P3V. 3A MAX CURRENT LIMIT
VADJ. 2A MAX CURRENT LIMIT. 1.2V TO 3.3V.

MISSING THE CLOCK, AND INTERRUPTION



EEPROM REQUIRED IN VITA57.1 STANDARD.
I2C LINE PULL-UP RESISTORS ON FPGA BOARD.
I2C ADDRESS SET BY CONTROLLER BOARD.

IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST
BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN

BOARD PRESENT PIN (H2) MUST
ALWAYS BE TIED TO GROUND

PINS MUST BE ASSIGNED STARTING WITH LA00 AND
MOVING UP THE LA BUS UNTIL IT IS FULL. WHEN
SINGLE-ENDED SIGNALING IS USED, THE _P LINE
SHOULD BE USED BEFORE THE _N LINE OF THE SAME
PAIR IS USED.



SCHEMATIC

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: NA

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PTD ENGINEER
MIGUEL USACH

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02_068253

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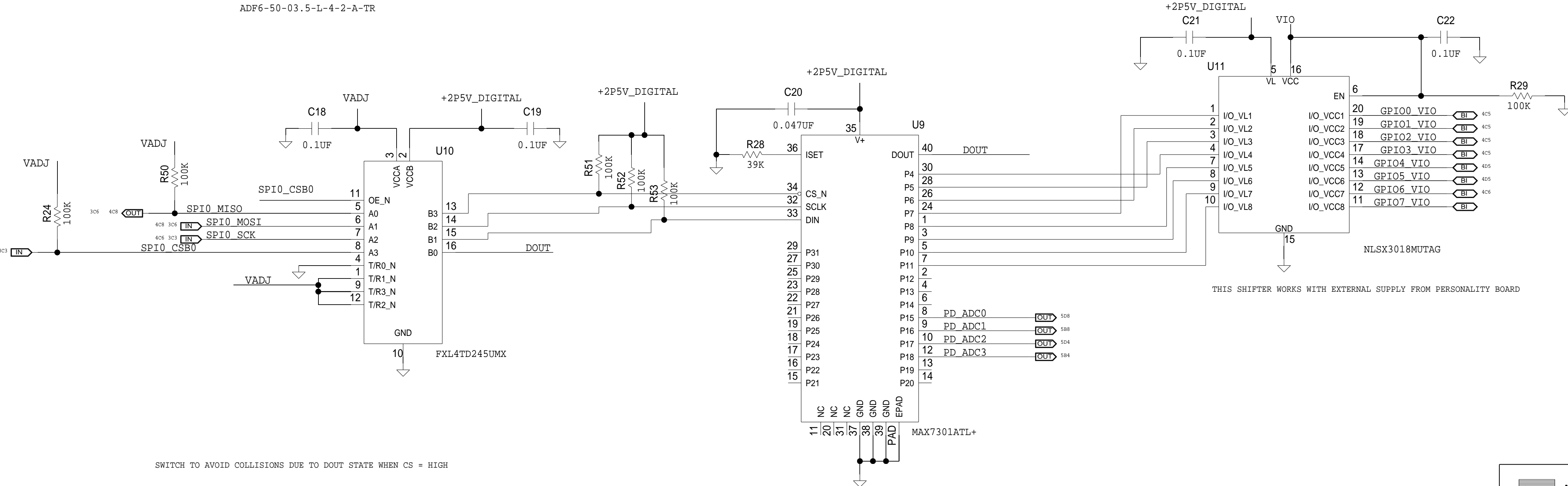
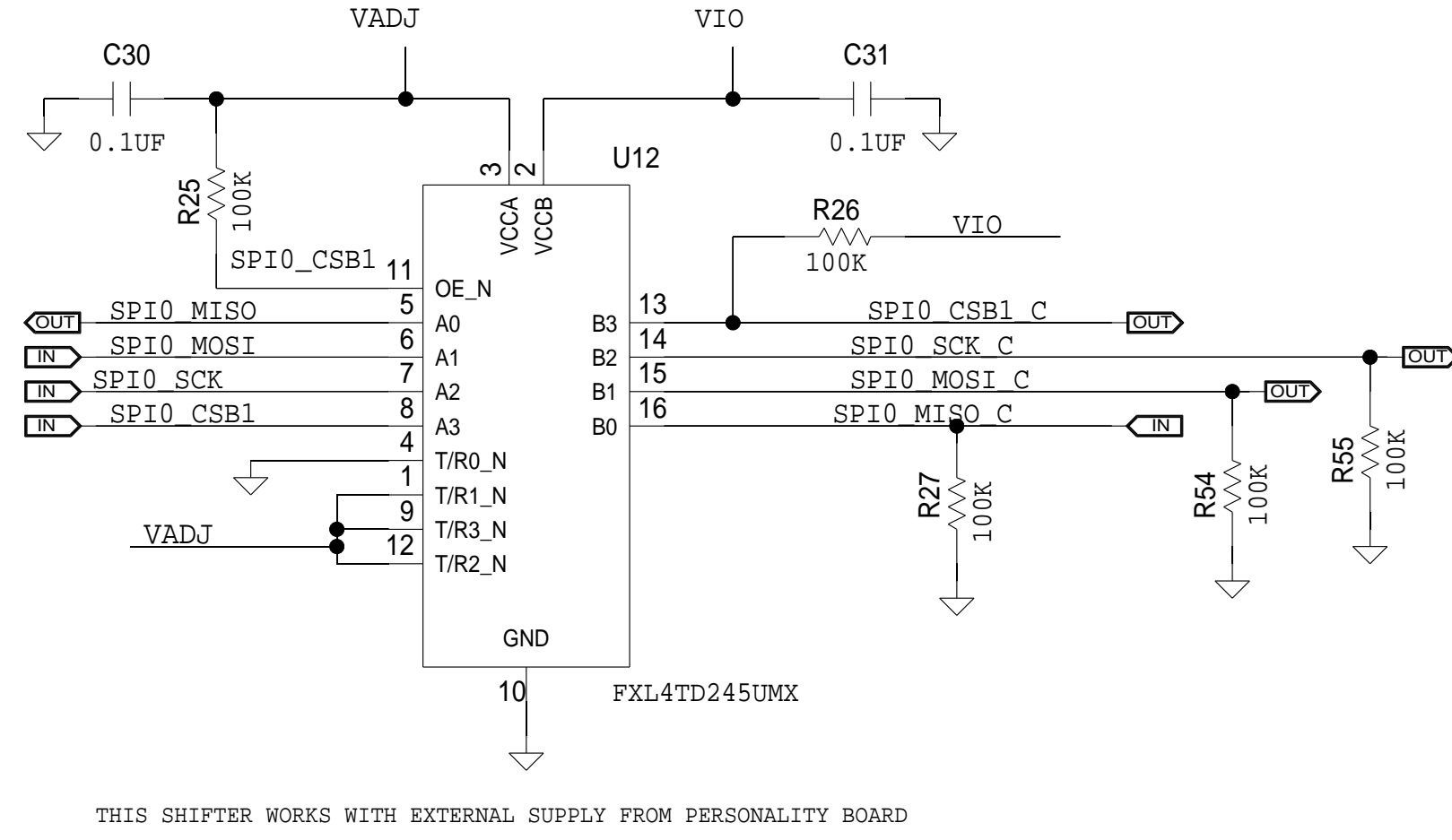
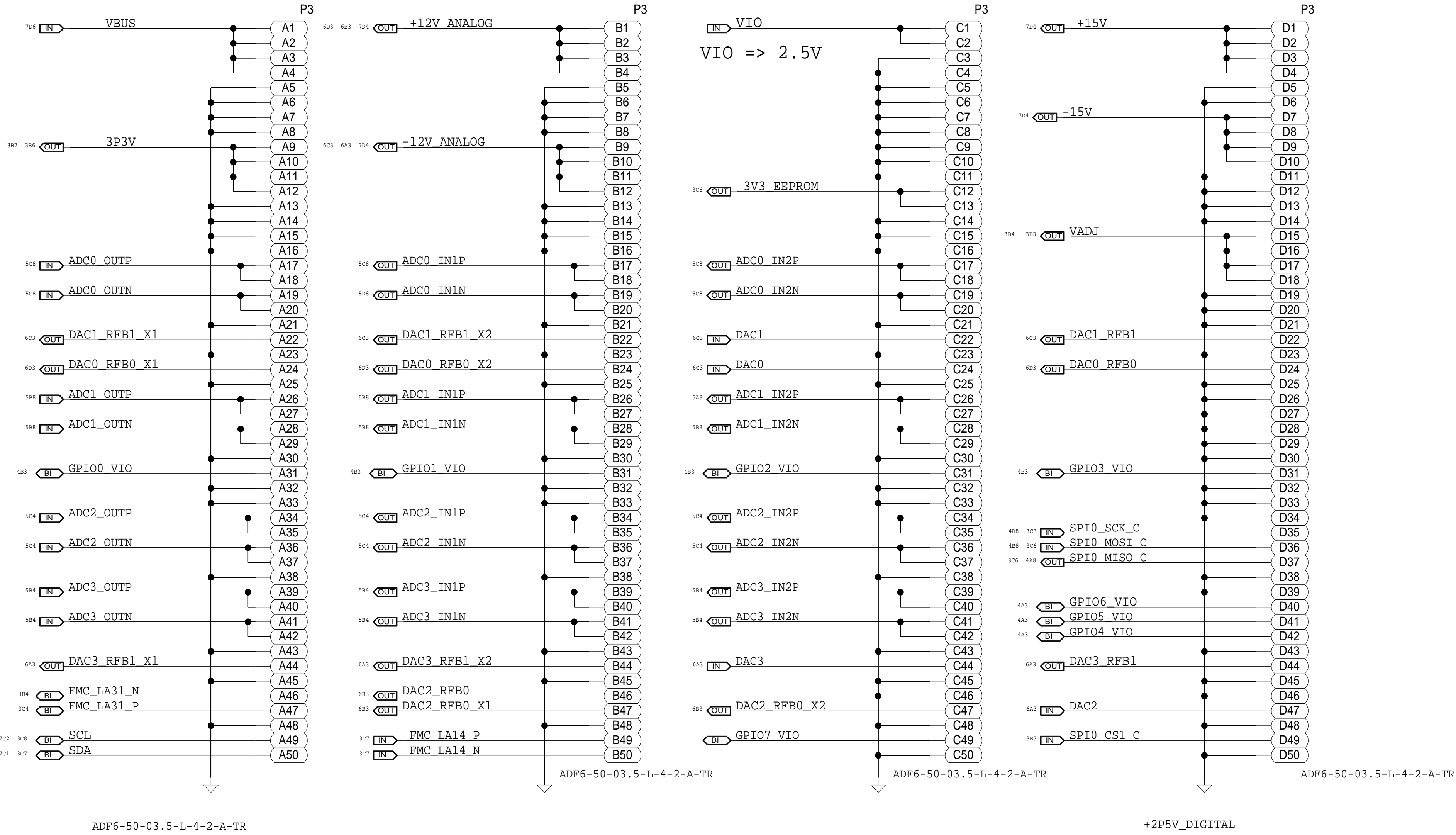
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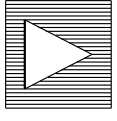
SHEET 3 OF 22

REV
B

MAXIMUM 1A CURRENT CONSUMPTION PER RAIL IN TEH PERSONALITY BOARD

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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LOW LATENCY I/O
Product(s): ADAQ237858
: NA

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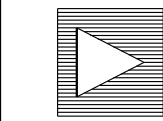
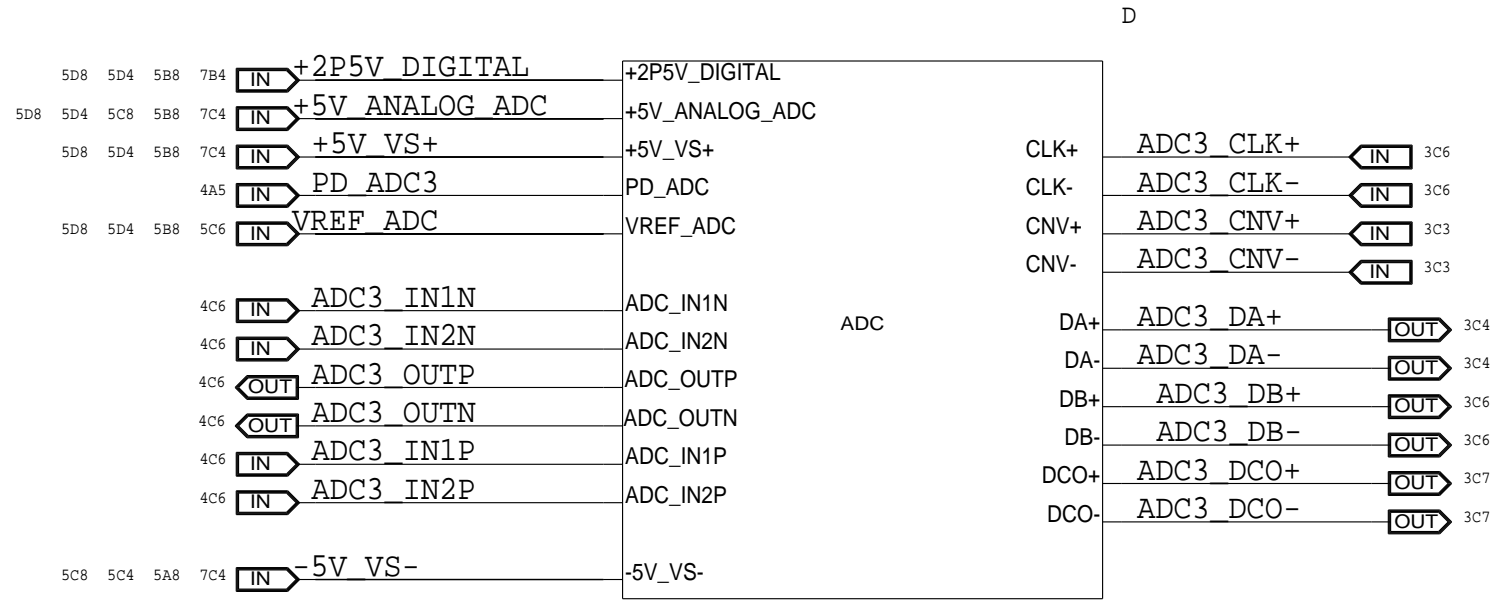
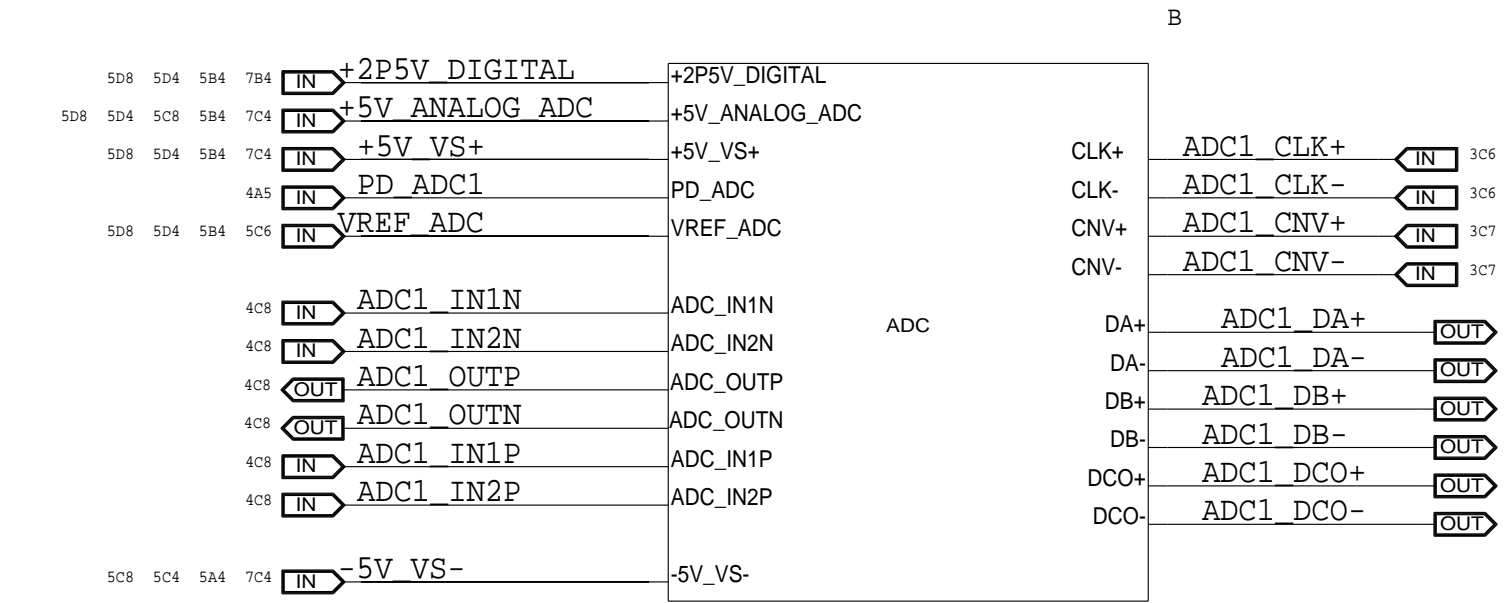
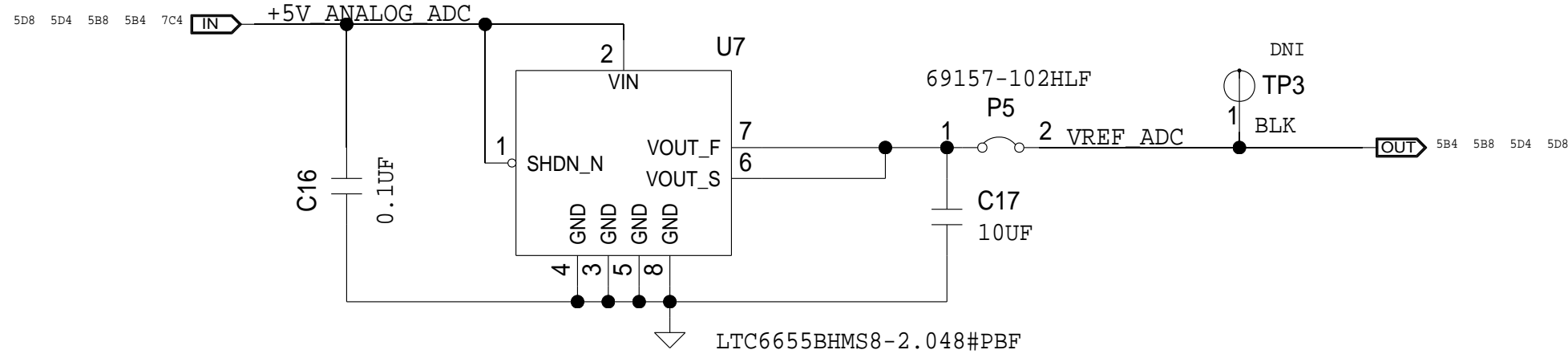
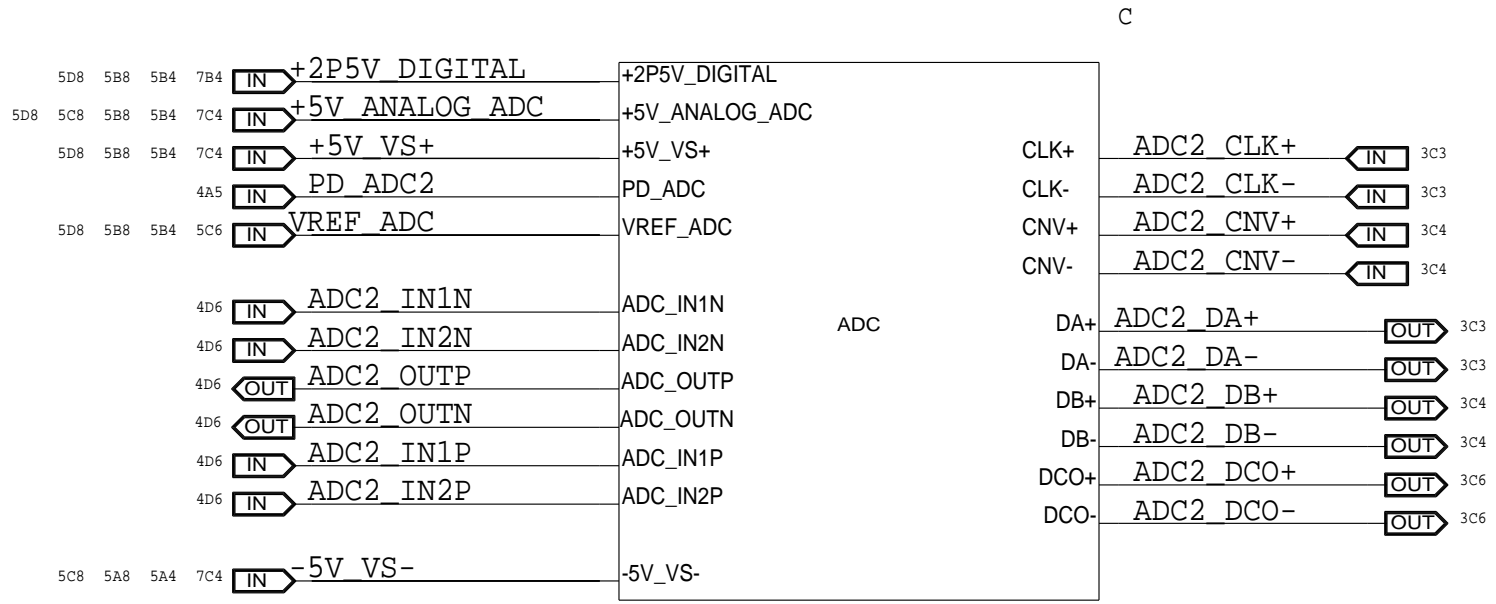
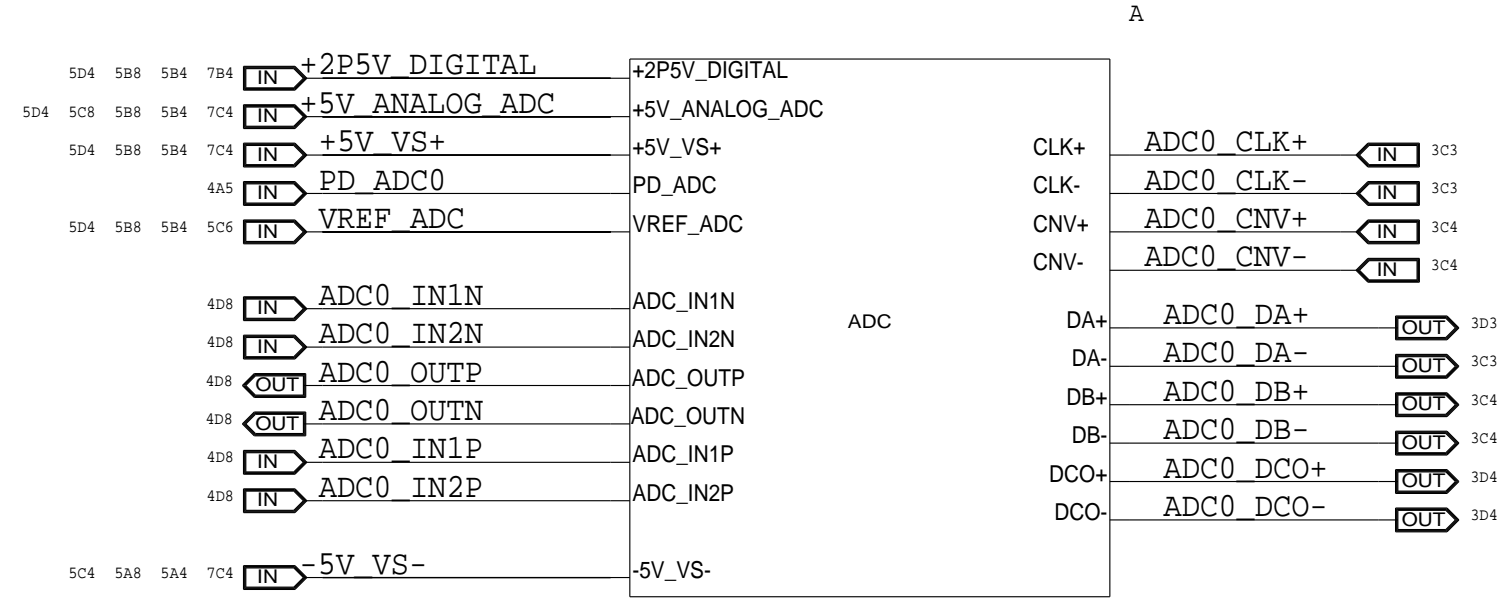
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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PTD ENGINEER
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REV
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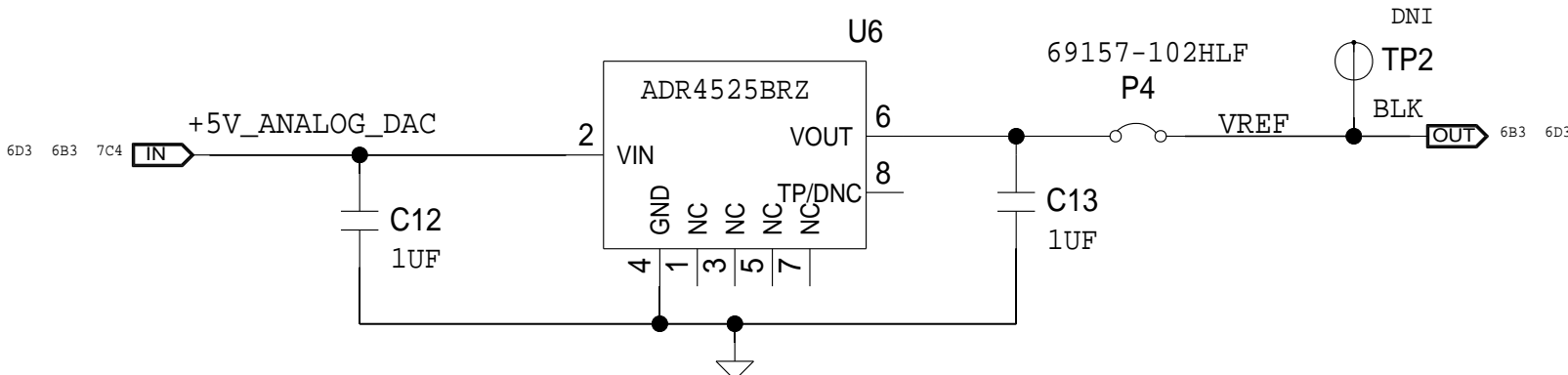
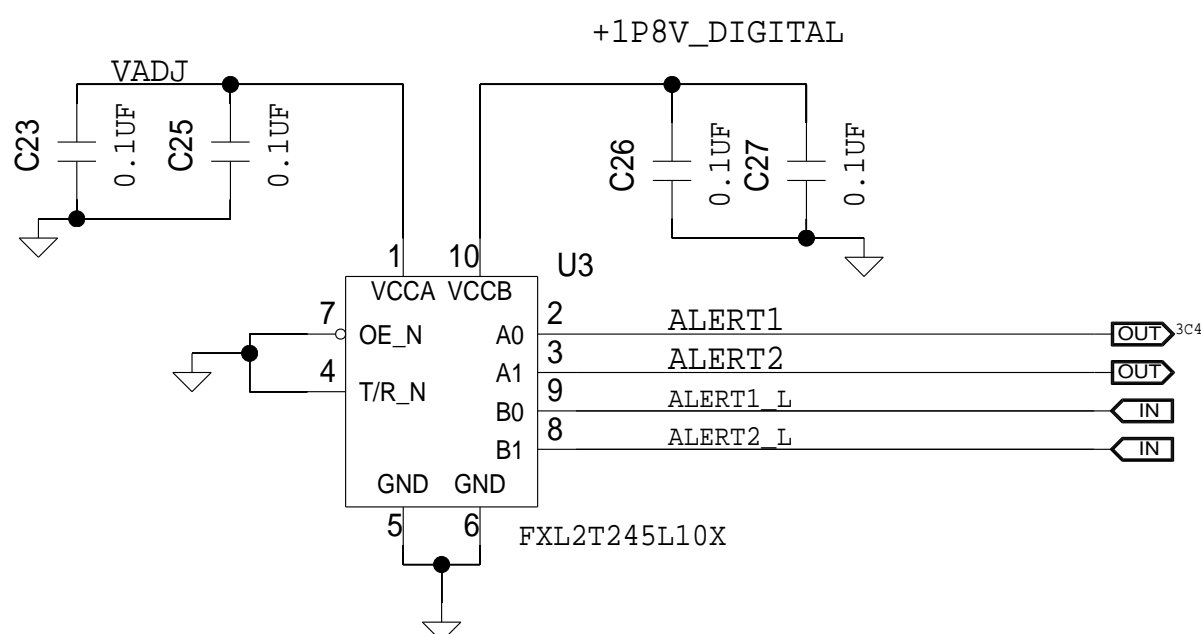
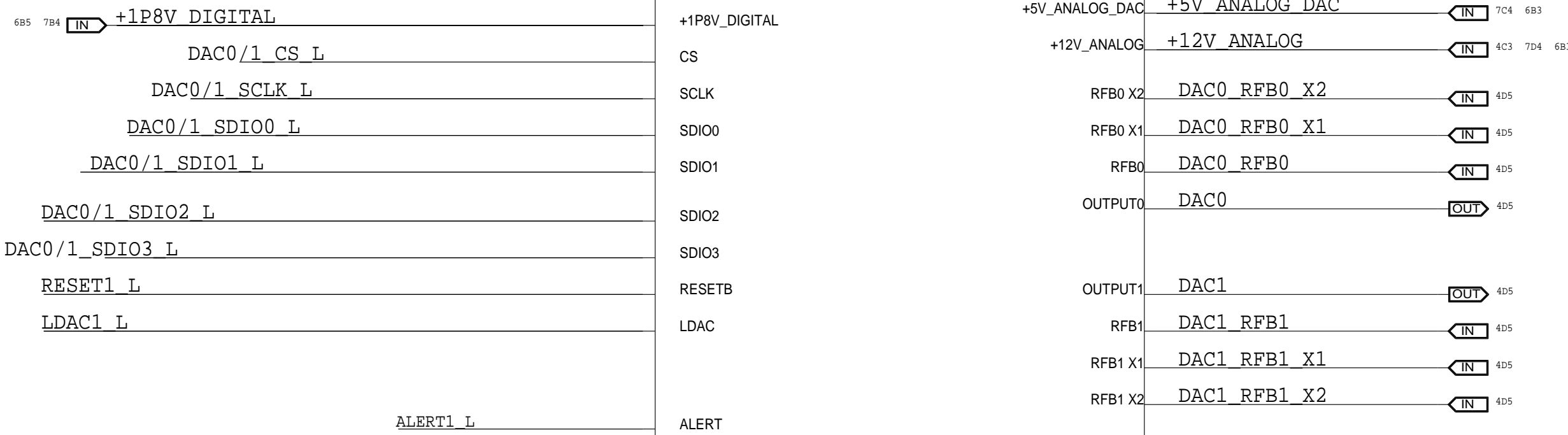
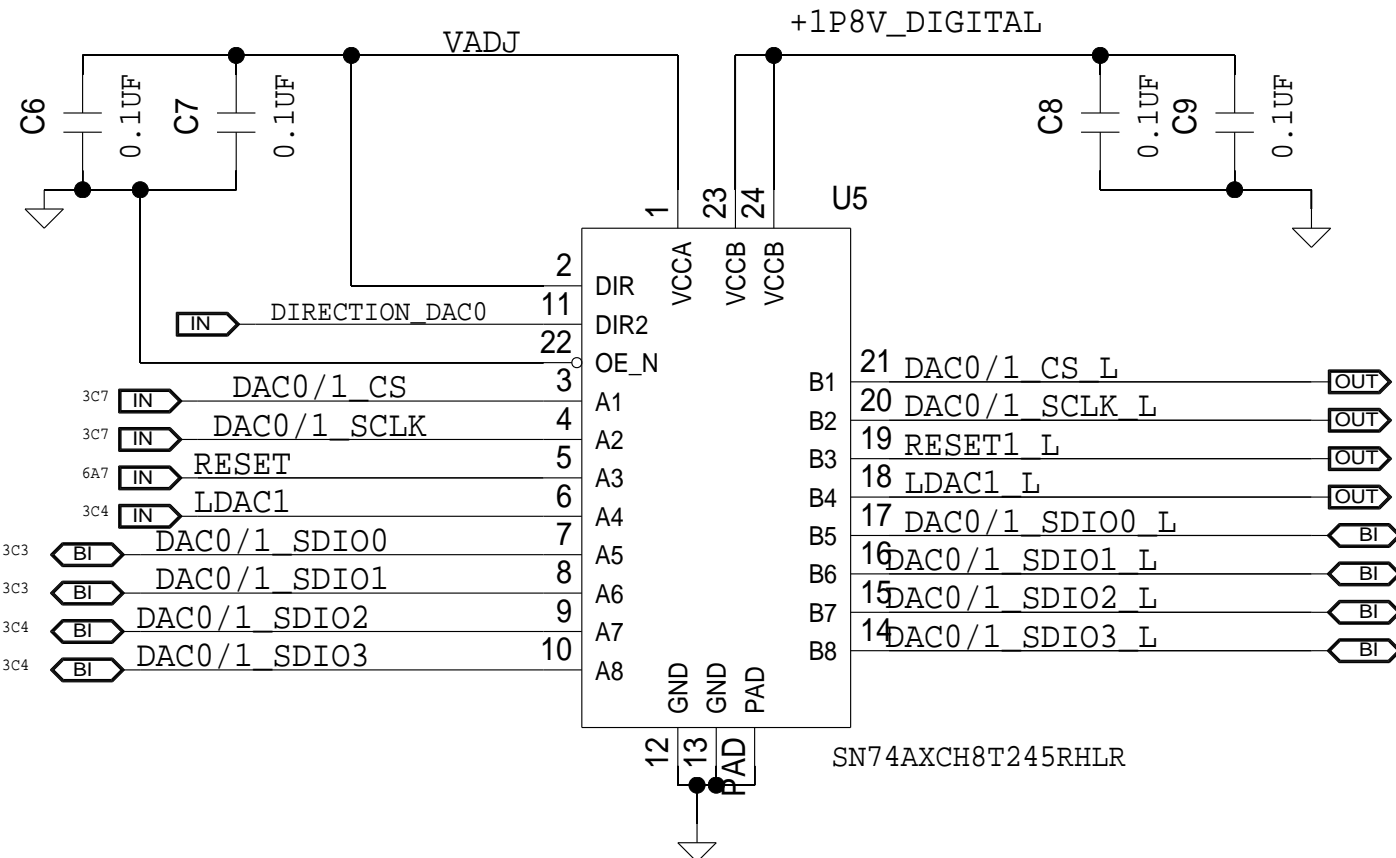
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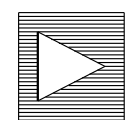
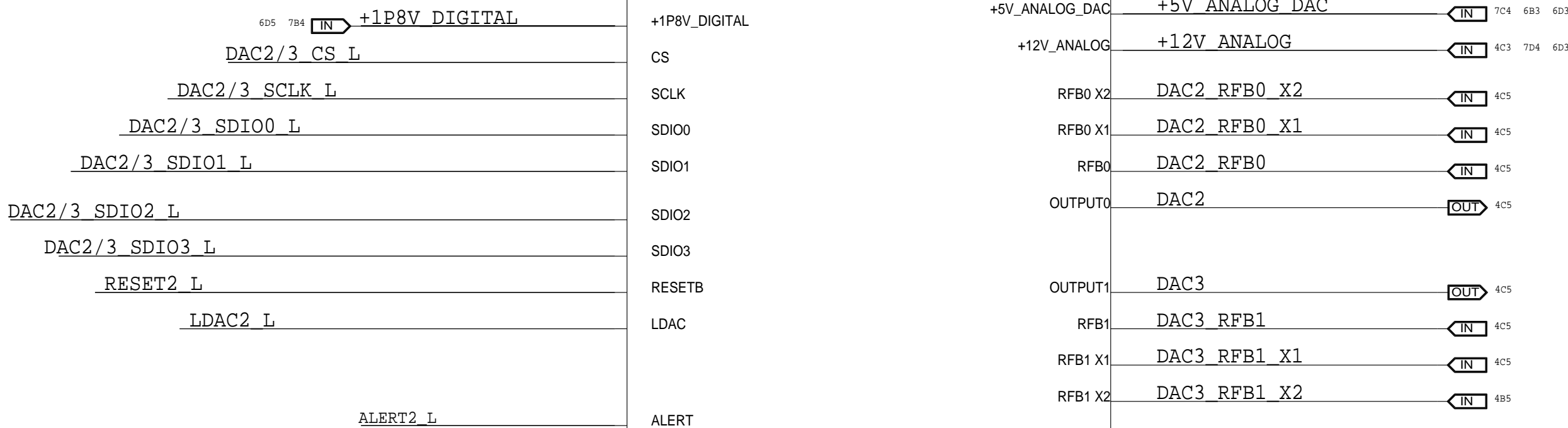
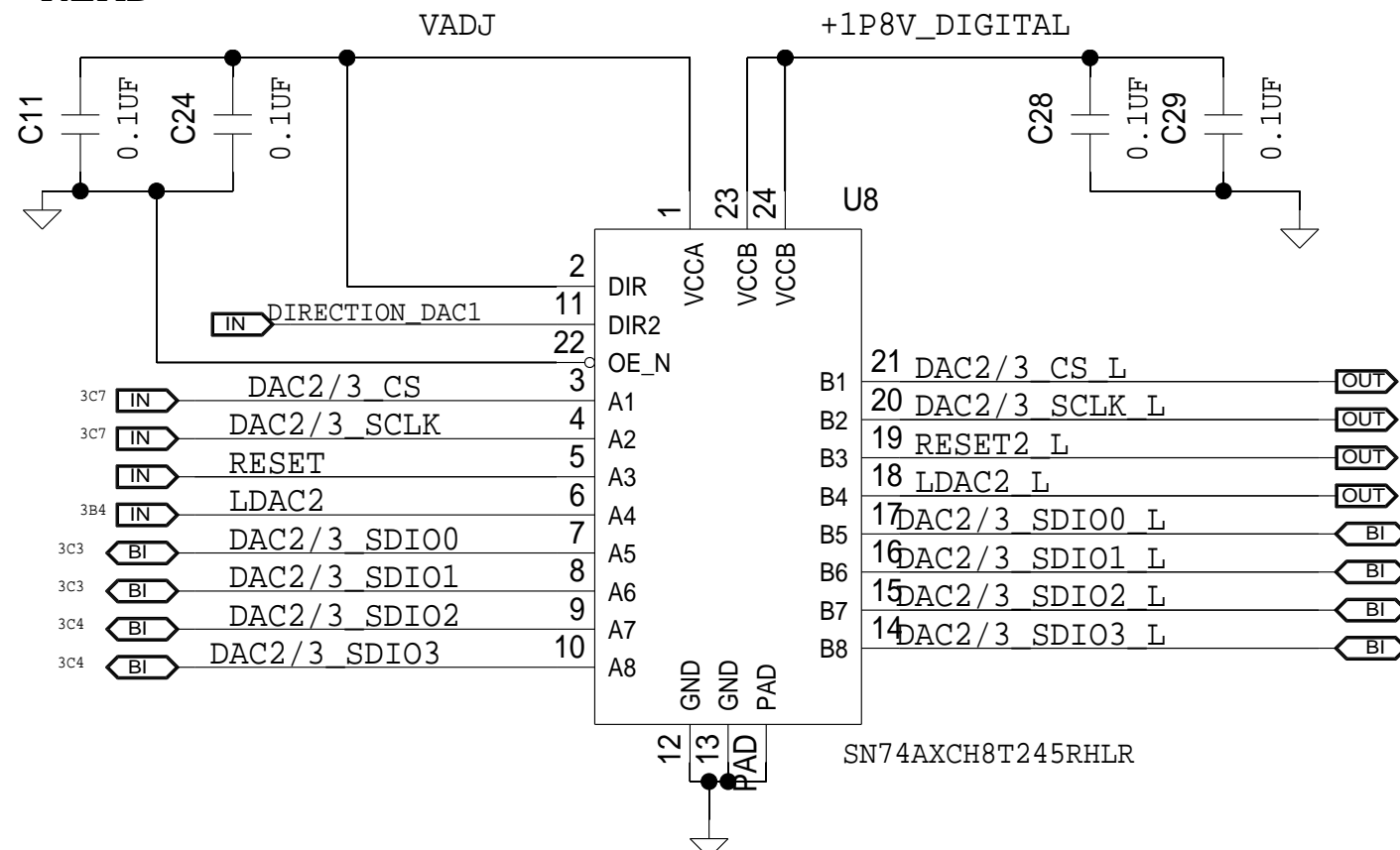
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DIRECTION
LOW -> WRITE
HIGH -> READ



DIRECTION
LOW -> WRITE
HIGH -> READ



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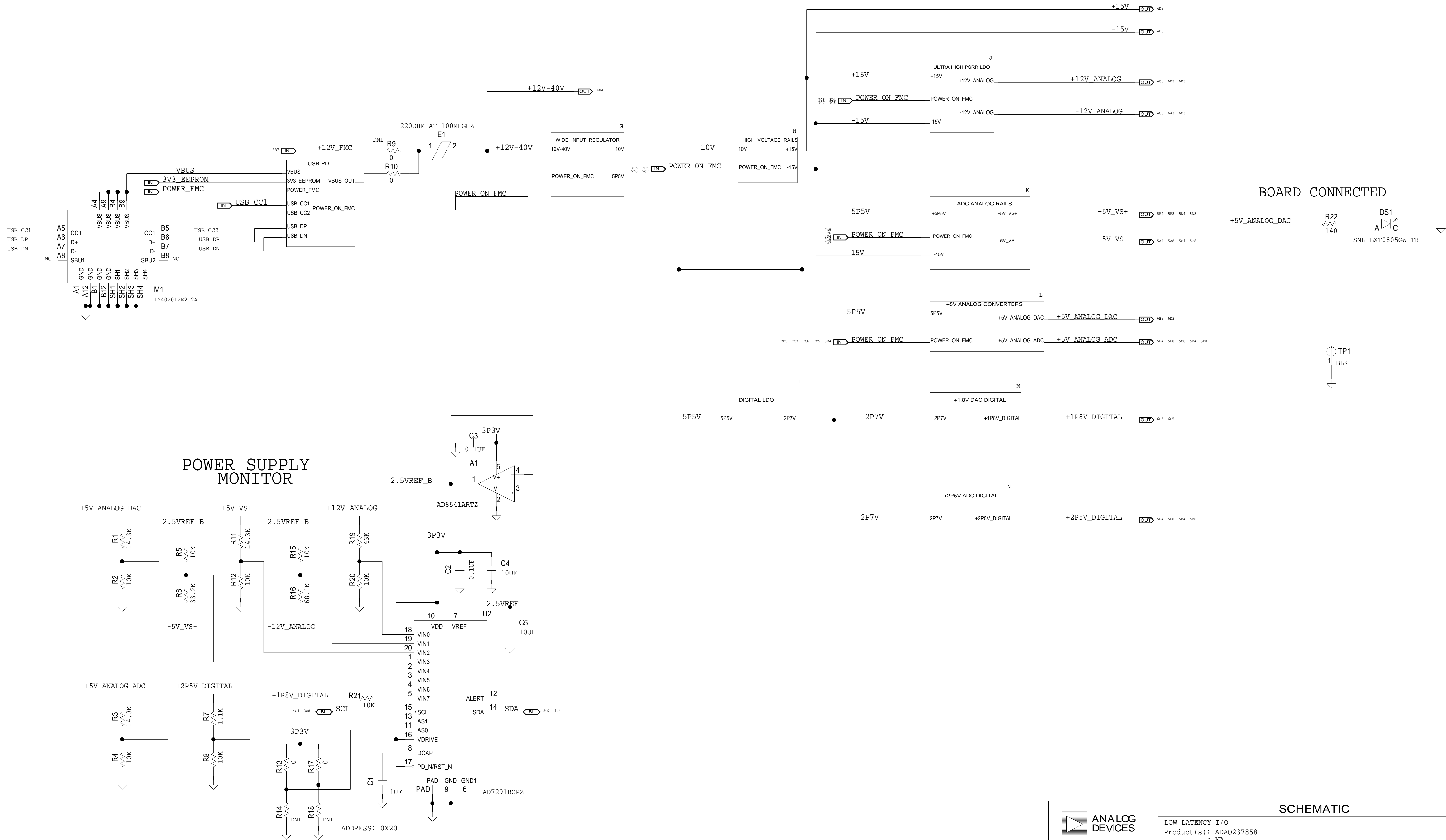
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REV
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
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PTD ENGINEER MIGUEL USACH	SIZE D	SCALE 1:1	SHEET 7 OF 22

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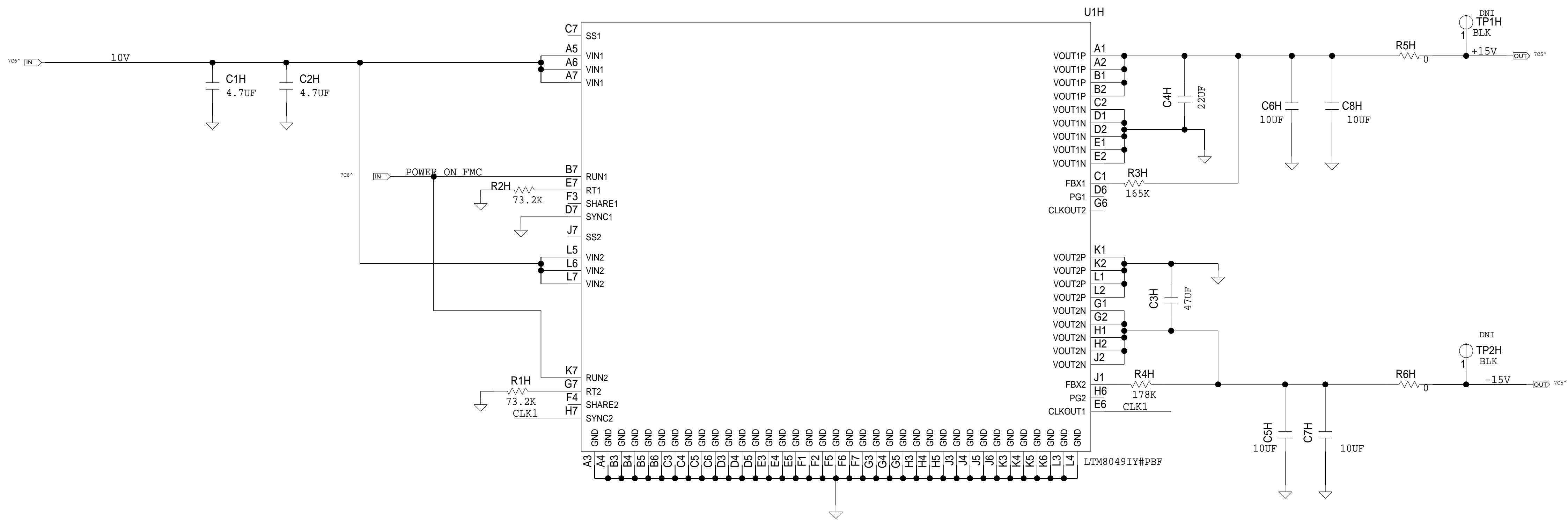
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REVISIONS

REV	DESCRIPTION	DATE	APPROVED



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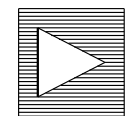
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02_068253

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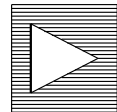
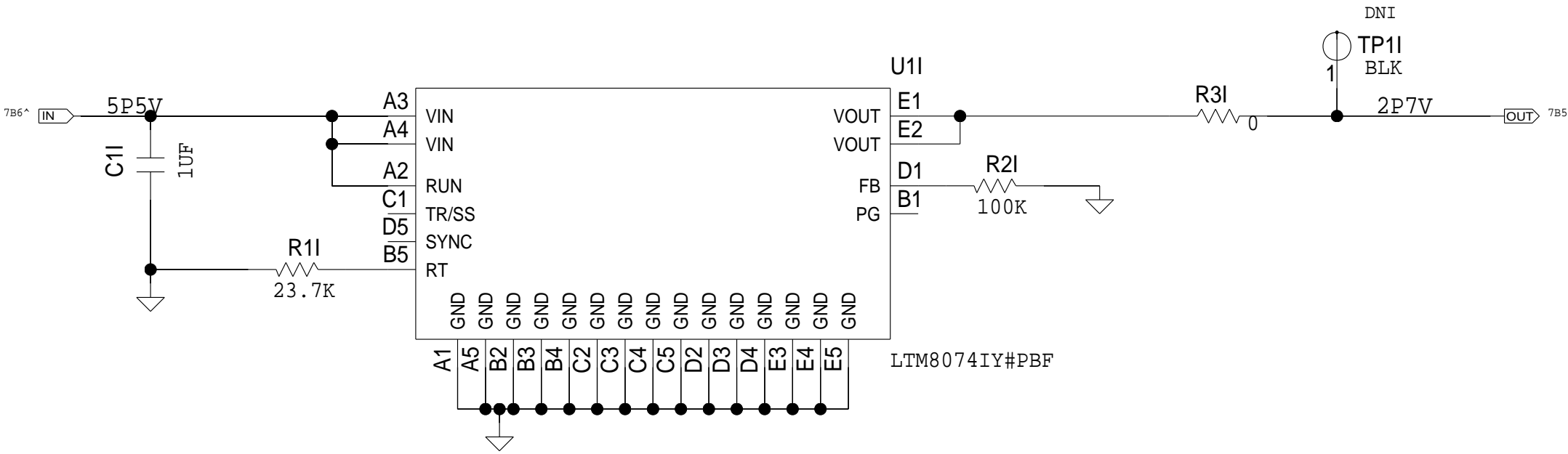
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: NA

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PTD ENGINEER
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REV
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SHEET 18 OF 22

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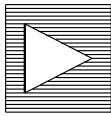
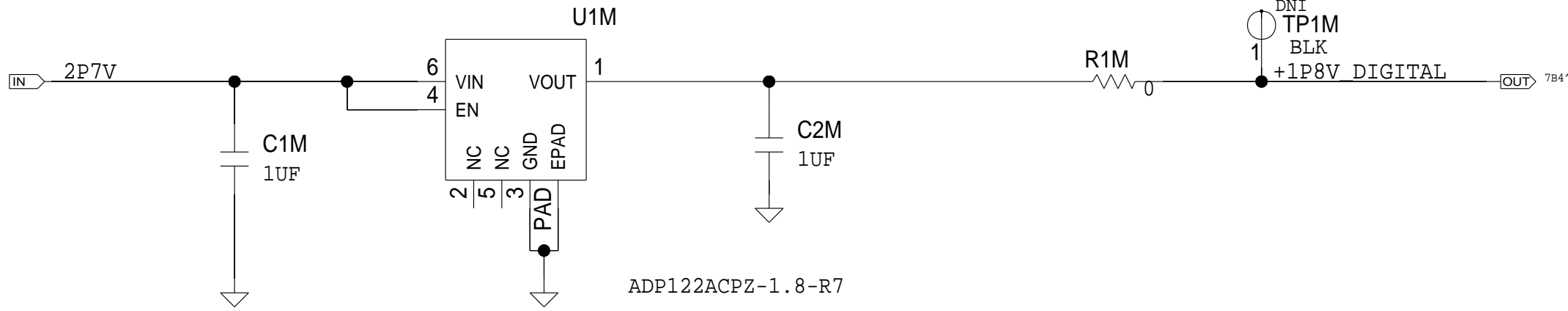
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REV	DESCRIPTION	DATE	APPROVED



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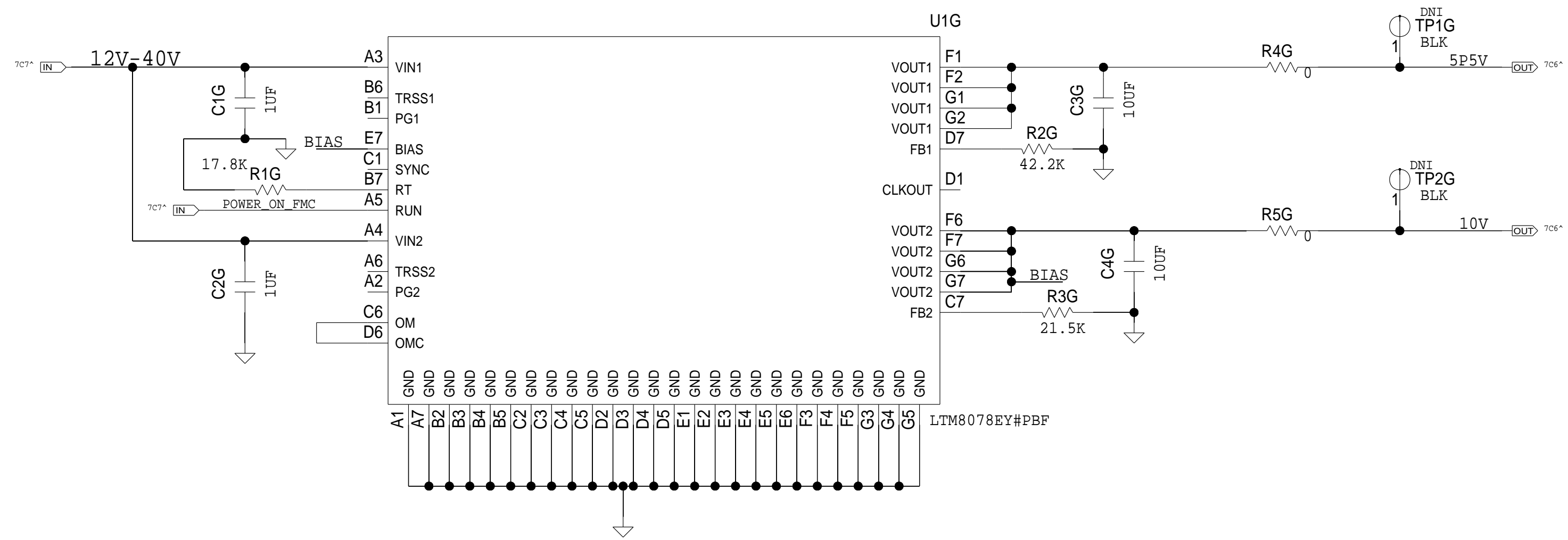
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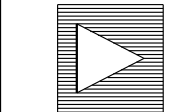
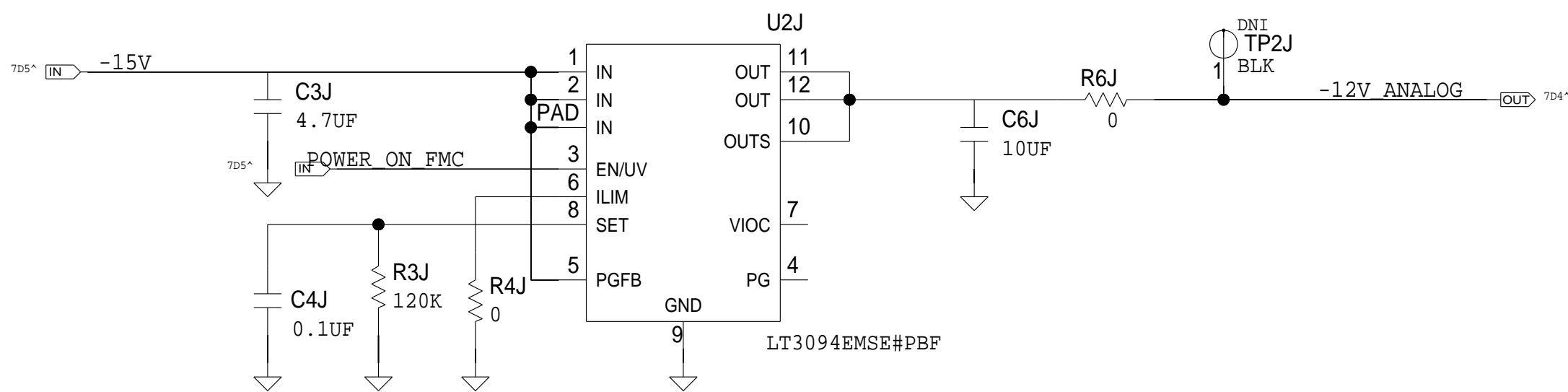
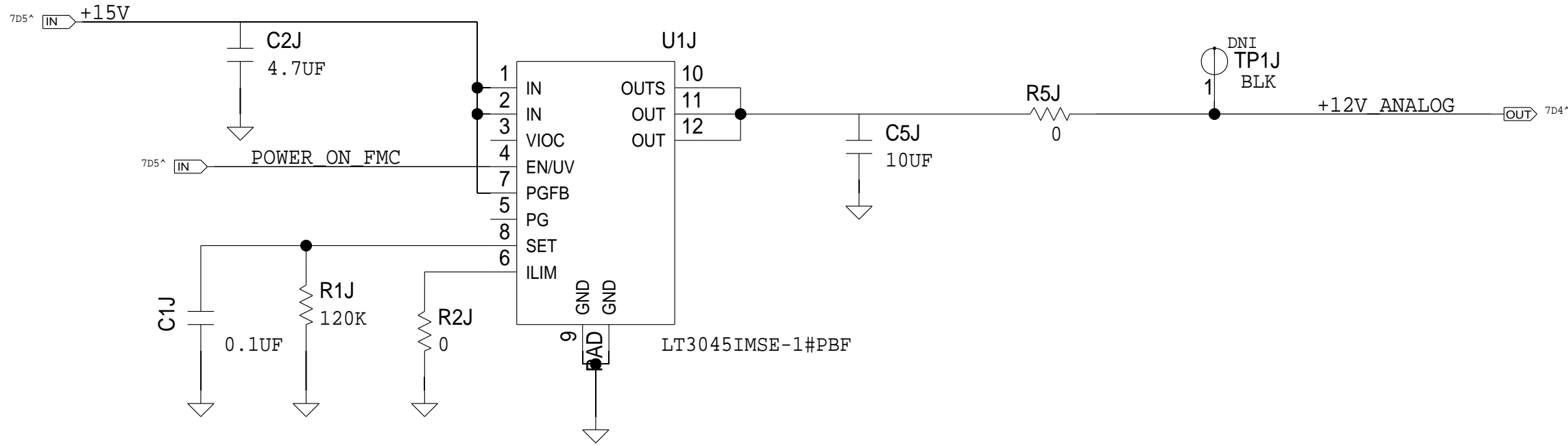
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02_068253

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